

SPECIFICATION

Passive Matrix LCD Module

(128 x 64 Dots)





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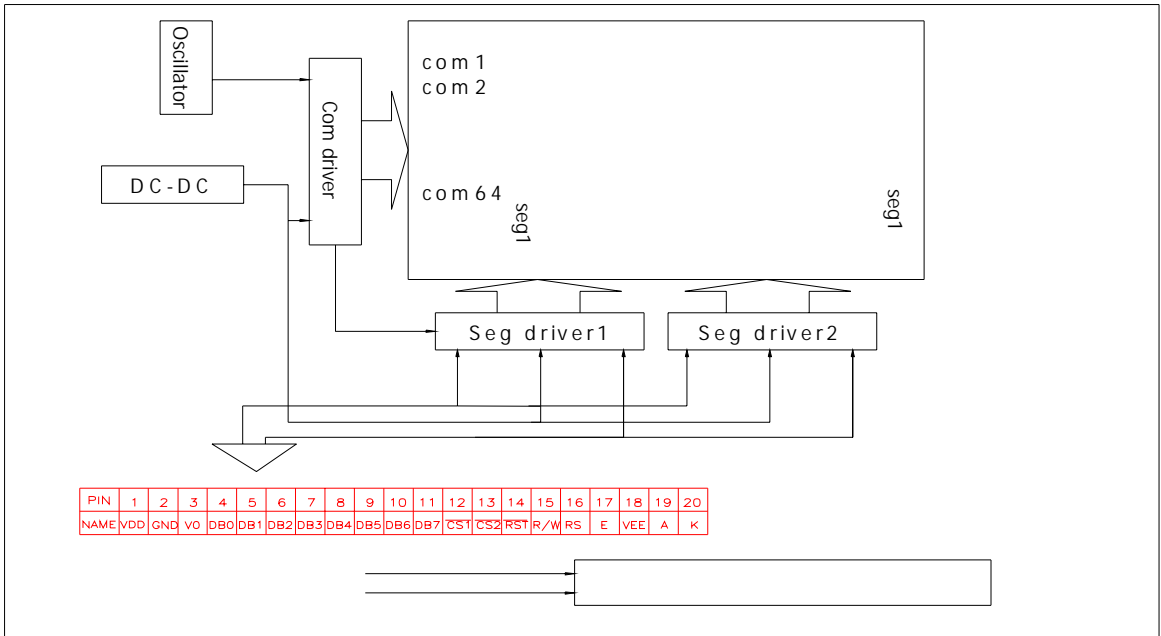
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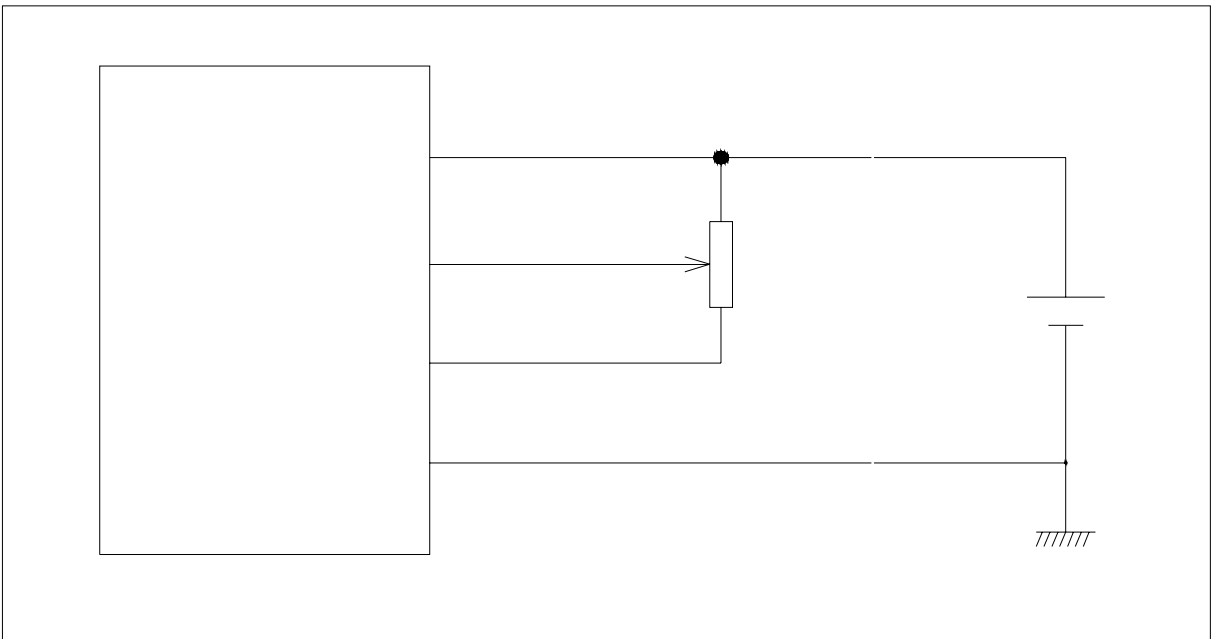
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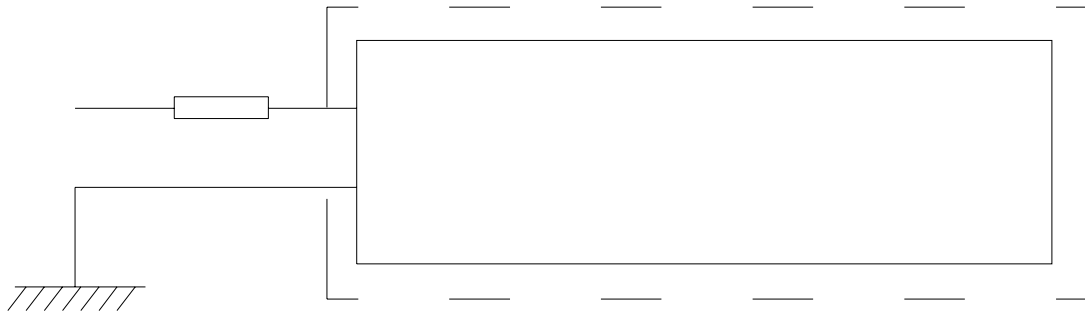
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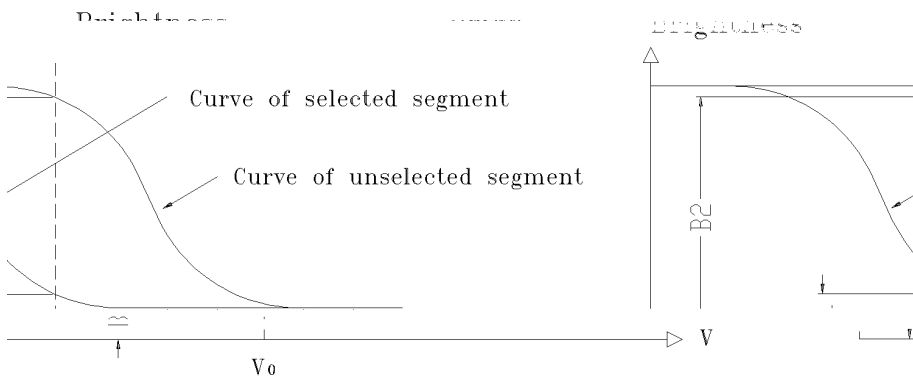
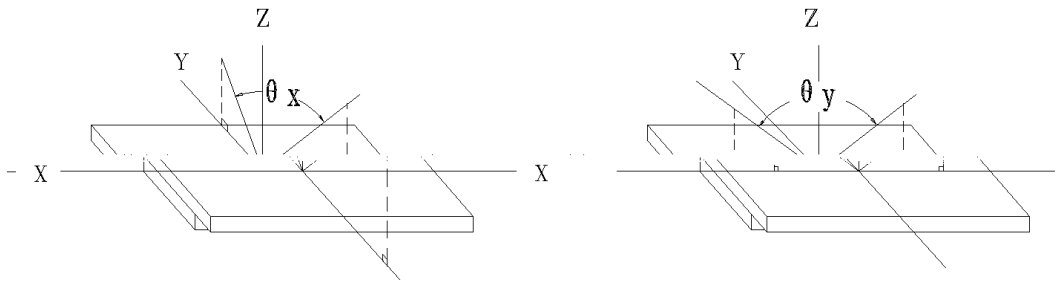
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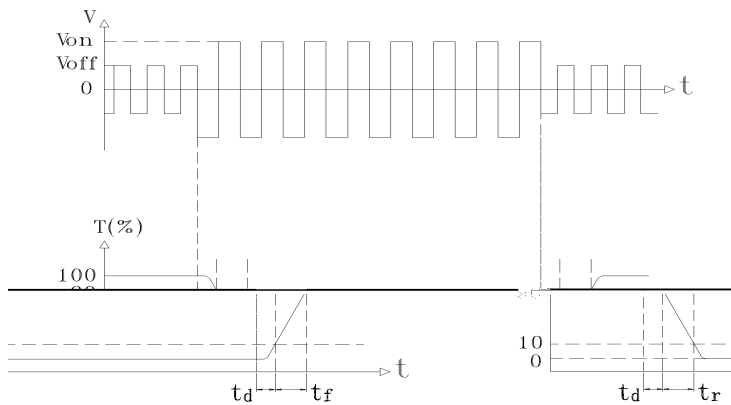


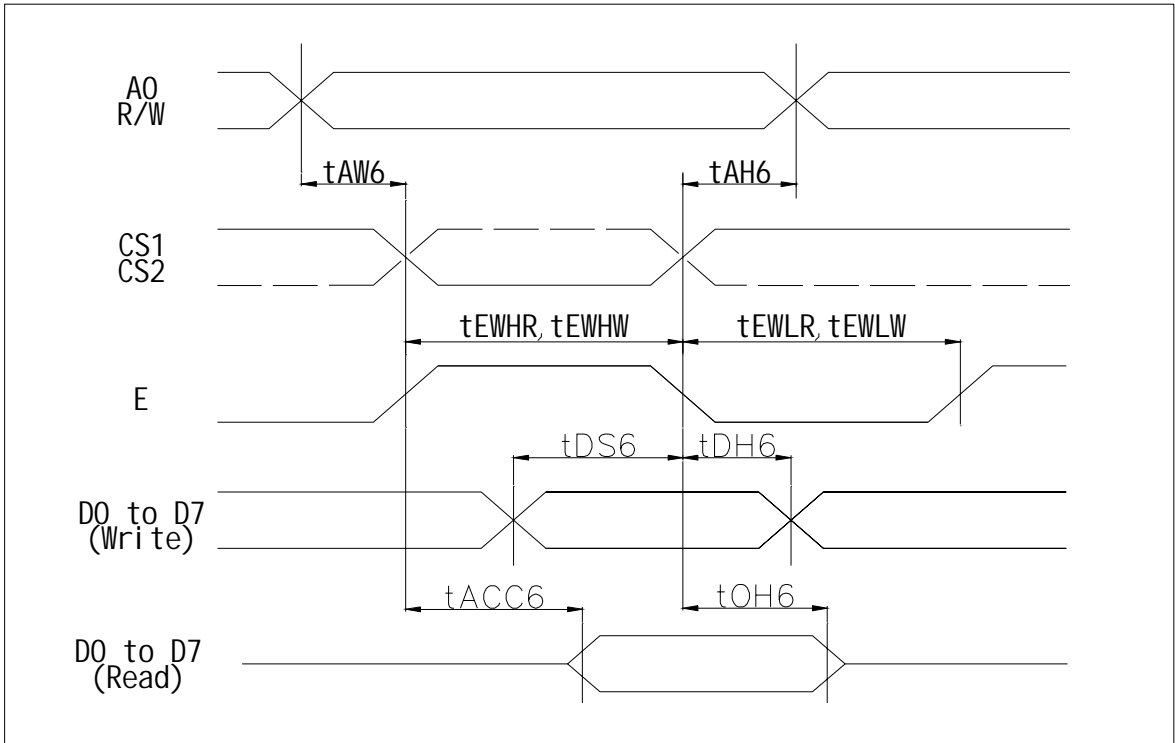
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$$\text{Contrast Ratio} = B2/B1 = \frac{\text{unselected state brightness}}{\text{selected state brightness}}$$





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The KS0108 chip identify the data bus signals by a combination of D/I, R/W, E signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only.

The interface is placed in a read mode when an “H” signal is input to the R/W terminal and placed in a write mode when a “L” signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. (See Timing Characteristics” regarding the timing.)

(1). Display ON/OFF

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0	Setting
0	0	0 0 1 1 1 1 1 0	Display OFF
			Display ON

(2) Display Start Line

Z address D5 - D0 (binary) of the display data RAM is set in the display start line register and is displayed at the top of the screen.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0	Line address
0	0	1 1 0 0 0 0 0 0	0
			1
			2
			↓
			62
			63

(3) Set Page (X Address)

X address D2 –D0 (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0	Page address
0	0	1 0 1 1 1 0 0 0	0
			1
			↓
			6
			7

(4) Set Y Address

Y address D5 - D0 (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0	Y address
0	0	0 1 0 0 0 0 0 0	0
		0 0 0 0 0 1	1
		0 0 0 0 1 0	2
		↓	↓
		1 1 1 1 1 0	62
		1 1 1 1 1 1	63

(5) Status Read

R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

BUSY	When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.
ON/OFF	Shows the liquid crystal display conditions: on condition or off condition. When on/off is 1, the display is in off condition. When on/off is 0, the display is in on condition.
RESET	RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted. RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

(6) Write Display Data

Writes 8-bit data D7 – D0 (binary) into the display data RAM. Then Y address is increased by 1 automatically.

R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

(7) Read Display Data

Reads out 8-bit data D7 – D0 (binary) from the display data RAM. Then Y address is increased by 1 automatically.

R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Read data							

Instructions	Command Code										Functions		
	R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0			
(1) Display ON/OFF	0	0	0	0	1	1	1	1	1	0	1	LCD display ON/OFF 1: ON, 0: OFF	
(2) Display start line	0	0	1	1	Display start line (0-63)							Specifies the RAM line displayed at the top of the screen.	
(3) Set page (X address)	0	0	1	0	1	1	1	Page (0-7)				Sets the page (X address) of RAM at the page (X address) register.	
(4) Set Y address	0	0	0	1	Y address (0-63)							Sets the Y address in the Y address counter.	
(5) Status read	1	0	busy 0 on/off res 0 0 0 0										Reads the status. RESET 1: Reset 0: Normal ON/ OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
(6) Write Display data	0	1	Write data										Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM
(7) Read Display data	1	1	Read data										Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: Busy time varies with the frequency (f CLK) of $\phi 1$, and $\phi 2$. ($1/f CLK \leq T_{busy} \leq 3/f CLK$)